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A Single-Chip False Target Radar Image Generator for Countering Wideband Imaging Radars

Douglas J. Fouts, *Member, IEEE*, Phillip E. Pace, *Senior Member, IEEE*, Christopher Karow, and Stig R. T. Ekestorm

***Abstract*—This paper describes the theory, design, implementation, simulation, and testing of an ASIC capable of generating false target radar images for countering wideband synthetic aperture and inverse synthetic aperture imaging radars. The 5.5 × 6.1 mm IC has 81632 transistors, 132 I/O pins, and consumes 0.132 W at 70 MHz from a 3.3-V supply. An introduction to the application and operation of the ASIC in an electronic attack system is also presented. The false target image is fully programmable and the chip is capable of generating images of both small and large targets, even up to the size of an aircraft carrier. This is the first reported use of all-digital technology to generate false target radar images of large targets.**

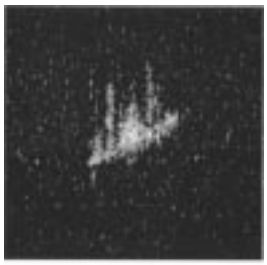
***Index Terms*—Digital image synthesis, digital signal processing, electronic warfare, inverse synthetic aperture radar, radar countermeasures, synthetic aperture radar, wideband imaging radar.**

I. Introduction

MODERN shipboard and airborne wideband synthetic aperture radars (SARs) and inverse synthetic aperture radars (ISARs) [1] are capable of generating images of target objects [2]–[4]. Fig. 1(a) and (b) (courtesy of the Tactical Electronic Warfare Division of the U.S. Naval Research Laboratory) shows a photograph of the USS Crockett and an image of the ship obtained from a U.S. Navy AN/APS-137 ISAR. Such imaging capability is an advantage over previous technology because it improves the ability to identify the specific type of target, distinguish friend from foe, accurately guide weaponry, and defeat electronic protection such as false target decoys [1], [5], [6]. Thus, modern wideband imaging SARs and ISARs create a difficult ship defense problem. For example, if an adversary is using a wideband imaging ISAR, an electronic protection system cannot synthesize a false target by simply transmitting a signal that emulates a radar return off a single or a few scattering surfaces. Instead, such a transmitted signal must emulate a coherent sequence of reflections with proper delay, phase, and amplitude that is similar to what would come from the multiple scattering surfaces at multiple ranges (distances from the radar) of an actual ship.

Analog methods for generating false radar targets have included the use of acoustic charge transport (ACT) tapped delay lines and fiber-optic tapped delay lines [7, Ch. 1]. ACT devices are no longer commercially available and also have limited bandwidth, making them impractical against wideband imaging radars [7, Ch. 1]. Optical devices are bulky and costly to manufacture, especially for the longer delay-line lengths needed to synthesize a false target image of even a moderately sized ship [7, Ch. 1]. However, the equations and algorithms needed to digitally synthesize a false target radar image have evolved considerably over the last several years [8]–[10]. With modern digital signal processing (DSP) techniques and advanced VLSI fabrication processes, it is now possible to digitally synthesize a realistic false target radar image of even a large war ship such as an aircraft carrier.

(a)



(b)

Fig. 1. (a) USS Crockett. (b) Image of USS Crockett from a U.S. Navy AN/APS-137 inverse synthetic aperture radar.

A wideband chirp waveform from a modern SAR or ISAR has a complex signal that can be described by

$$s(t) = rect\left(\frac{t}{T}\right) e^{j2\pi(f_c t + (Kt^2)/2)} \tag{1}$$

$$rect\left(\frac{t}{T}\right) = \begin{cases} 1 & for \quad \left|\frac{t}{T}\right| < \frac{1}{2} \\ 0 & for \quad \left|\frac{t}{T}\right| > \frac{1}{2} \end{cases} \tag{2}$$

$$K = \frac{\Delta}{T} \tag{3}$$

where t is time, T is the pulsewidth, f_c is the carrier frequency, K is the chirp rate, and Δ is the linear frequency sweep or

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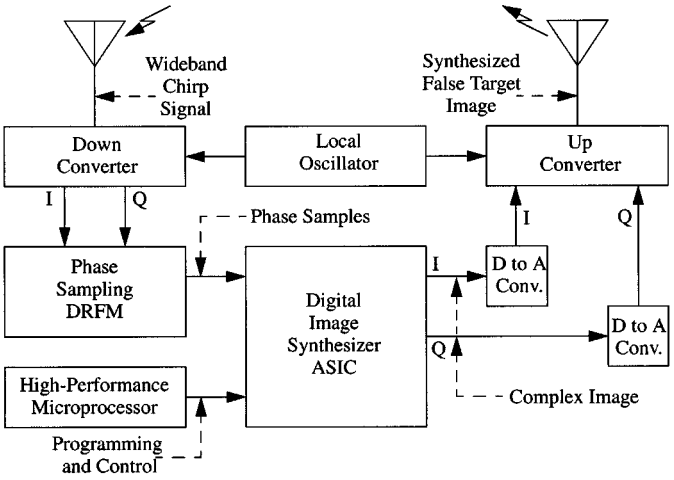

Fig. 2. Block diagram of the false target radar image synthesizer system.

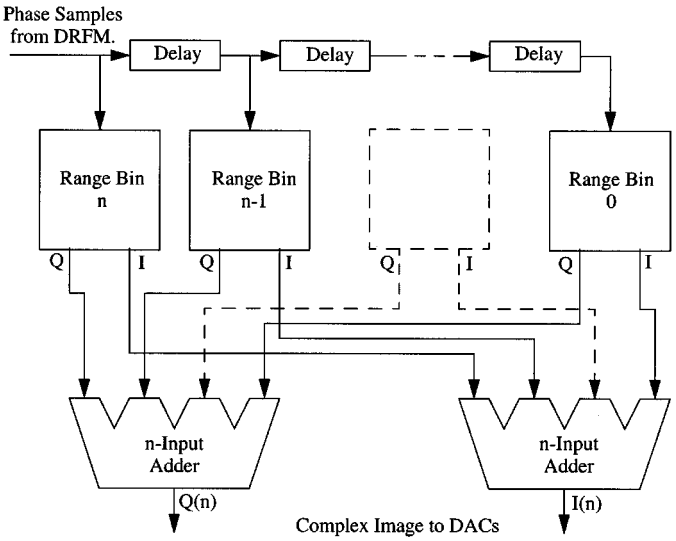

Fig. 3. Virtual architecture of the digital image synthesizer.

the bandwidth of the transmitted signal [11]. With the interception of such a signal, a realistic false target radar image can be digitally synthesized using the system shown in Fig. 2, which makes use of high-performance digital radio frequency memory (DRFM), analog-to-digital converter (ADC), digital-to-analog converter (DAC), and microprocessor (μ PC) technology [12]. However, the heart of the system is the full-custom all-digital ASIC described in this paper, which is referred to as the digital image synthesizer (DIS). Referring to Fig. 2, the received wideband chirp waveform, which is sometimes referred to as a radar pulse, is downconverted to baseband as described by

$$s(t) = \text{rect}\left(\frac{t}{T}\right) e^{j2\pi(f_{\text{d}}\text{PRI}+(Kt^2/2))} \tag{4}$$

where f_{d} is the Doppler frequency between the radar and the DIS platform intercepting the chirp signal, and PRI is the pulse repetition interval [12]. The Doppler shift is only tens of Hertz compared to the megahertz chirp bandwidth. Therefore, a constant phase change within a chirp pulse can be assumed. After sampling and digitization, the phase samples are used by the DIS to synthesize a complex false target image. This image is then converted back to an analog signal, applied to the upconverter, and amplified for transmission back to the radar. The entire system operates under control of the microprocessor, which also programs the DIS with the parameters necessary to synthesize the false target image(s) desired by the system operator.

II. Digital Image Synthesizer Architecture

Fig. 3 illustrates the virtual architecture of the DIS [7, Ch. 3]. The phase samples of the radar pulse are read out of the DRFM and propagate through a cascade of delays that represent the delays between the different range bins. Each range bin can synthesize a radar return signal from one or more emulated scattering surfaces as long as all surfaces are in the same range bin, or at the same range, or distance, from the radar. The use of multiple range bins with delay between each range bin allows the synthesized false target to have many scattering surfaces at many different ranges, an especially necessary feature if the synthesized false target image is that of a large ship. The outputs of all range bins are then summed together before being applied to the DAC and upconverter.

The signal processing that occurs in the DIS is described by

$$I(n) = \sum_{i=0}^{E} A_i \cos\left(\phi(n-i) + \Delta\phi_i\right) \tag{5}$$

$$Q(n) = \sum_{i=0}^{E} A_i \sin\left(\phi(n-i) + \Delta\phi_i\right) \tag{6}$$

where E is the extent of the false target image or the number of range bins used to generate the image, A_i is the magnitude scaling factor for range bin i, $\phi(n)$ is the delayed input phase sample from the DRFM, and $\Delta\phi_i$ is the phase rotation coefficient for range bin i [7, Ch. 2], [12]. Within a range bin, the creation of Doppler modulation requires rotating the phase of the incoming sample. Then, the phase sample must be converted to a complex (I, Q) signal. Next, amplitude modulation within each range bin is used to account for the radar cross section of the scattering surface being emulated. Finally, the signals from the different range bins are summed together to generate the composite return signal. Fig. 4 shows the virtual architecture of an individual range bin. Note that the amount of phase rotation and the amount of amplitude scaling can be individually programmable for each range bin by the control microprocessor, giving the DIS extreme flexibility in generating an almost infinite variety of false target radar images.

III. Design of the Digital Image Synthesizer ASIC

The architecture shown in Figs. 3 and 4 has a major implementation problem in that the summation adders must sum as many as 128–512 inputs to synthesize a practical-sized target. Parallel adders of this size are not feasible even with modern VLSI technology. A multiple-level adder with multiple inputs would need to be used, such as a carry–save adder or a Wallace-tree adder [13]. However, these types of adders with 128–512 inputs would require a large number of logic delays to sum together all the outputs of all the range bins and would thus be excessively slow, even if pipelined to improve speed.

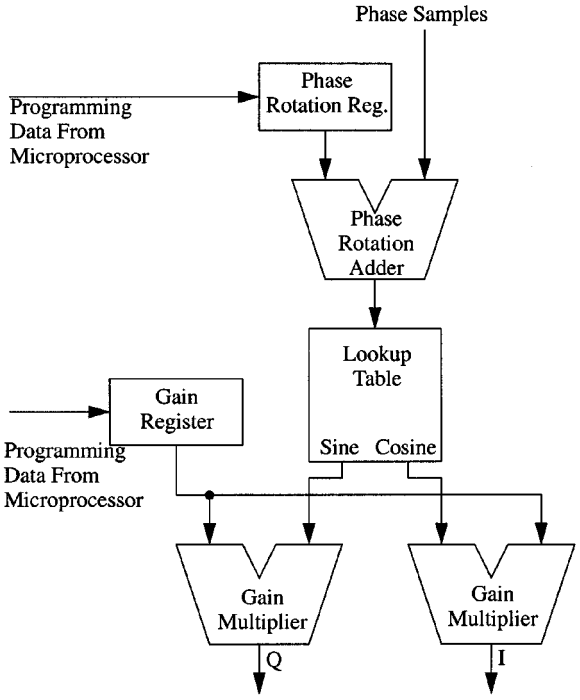

Fig. 4. Range bin virtual architecture.

In the DIS implementation described here, the bottleneck is solved by taking advantage of the fact that processing within each range bin is independent of the delay between range bins. The delay can be applied either to the DRFM sample before the sample is processed by the range bin or to the output of the gain multiplier before it is summed with the outputs of other multipliers from other range bins. By applying the delay at the output of the gain multiplier and by using a pipelined cascade of two-input adders with the delay through each addition stage matched to the required delay between range bins, the need for an explicit delay element between range bins can be eliminated. This not only improves speed but also reduces the required number of transistors because of the elimination of the dedicated explicit delay elements between range bins shown in Fig. 3. The architecture of the actual DIS implementation is shown in Fig. 5. The architecture of the actual range-bin implementation is shown in Fig. 6.

Referring to Fig. 6, operation of the DIS starts when the control microprocessor (shown in Fig. 2) independently programs the phase rotation and gain for each range in. To improve performance, these inputs are double buffered to allow the control microprocessor to reprogram the DIS while the IC is still finishing calculations using previous programming. The phase rotation is a 4-bit unsigned number and both the phase rotation buffer and the phase rotation register are 4 bits wide. The gain data is 2 bits, allowing gain scaling by 1, 2, 4, or 8. The gain buffer and the gain register are 2 bits wide. After the gain and phase coefficients are loaded, a sequence of phase samples from the DRFM is clocked into each range bin. Each range bin loads the same phase sample on the same clock, as shown in Fig. 5, and processes the same phase sample on the same clock.

To further improve the performance of the DIS, the range-bin architecture shown in Fig. 4 has been heavily pipelined. The

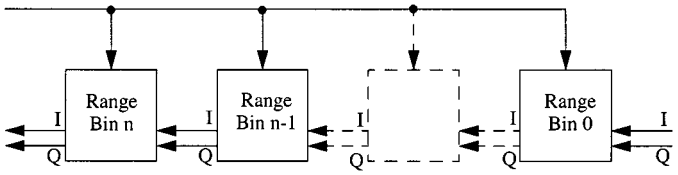

Fig. 5. Architecture of DIS implementation.

addition of four pipeline stages, as shown in Fig. 6, maximizes computational throughput at the cost of increased computational latency and additional hardware. The phase samples from the DRFM are added to the value in the phase rotation register and the result is stored in a pipeline register. The samples from the DRFM are 5 bits wide and the phase rotation adder is 5 bits wide, but the phase increment value is only 4 bits wide. At the sacrifice of 1 bit of phase precision, the phase rotation value is shifted left 1 bit before the addition. Thus, the phase rotation adder implements a modulo-32 addition and ignores overflow. Overflow can be ignored because both the sine and cosine operations that follow are periodic functions.

The output of the phase rotation adder is applied to the combined sine/cosine ROM lookup table, via the indicated pipeline register. The ROM has five address lines and thus 32 words. Both the sine and the cosine outputs have 8 bits, thus the ROM has 16 bits at each address. The sine and cosine outputs use a two's complement format that consists of seven fractional data bits and one sign bit. The outputs of the ROM go to two 8-bit pipeline registers.

The sine and cosine ROM outputs are connected to the gain multipliers via the indicated pipeline registers. The gain multipliers have full-range 11-bit outputs, but are not true arithmetic multipliers. The multiplication is actually accomplished by shifting. This is feasible because the 2-bit gain data represents signed multiplication by 1, 2, 4, or 8, which equates to 18 dB of dynamic range. Multiplication using a shifter instead of an actual arithmetic multiplier greatly increases the performance of the DIS and reduces the number of transistors at the same time. The output of each shifter goes to an 11-bit pipeline register.

After multiplication, the data from each range bin is added to the data from all the other range bins. This is accomplished using a cascade of two-input pipelined adders. Referring to Fig. 6, the I and Q partial summation inputs to the adders come from the outputs of the summation adders in the previous range bin, except for the range bin at the far right side of the cascade of range bins in Fig. 5. For this range bin, the summation adder inputs are 0. The outputs of the summation adder in each range bin are connected to the partial summation inputs of the summation adder in the following range bin, except for the range bin on the far left side of the cascade of range bins in Fig. 5. The summation adder outputs for this range bin are the primary outputs of the DIS that go to the DAC. The summation adders are 16-bit ripple-carry two's complement adders. This allows up to 32 range bins to be cascaded together without risk of arithmetic overflow. In an actual system, many more than 32 range bins can actually be cascaded because at any given time, approximately half of the range bins will be generating negative partial results.

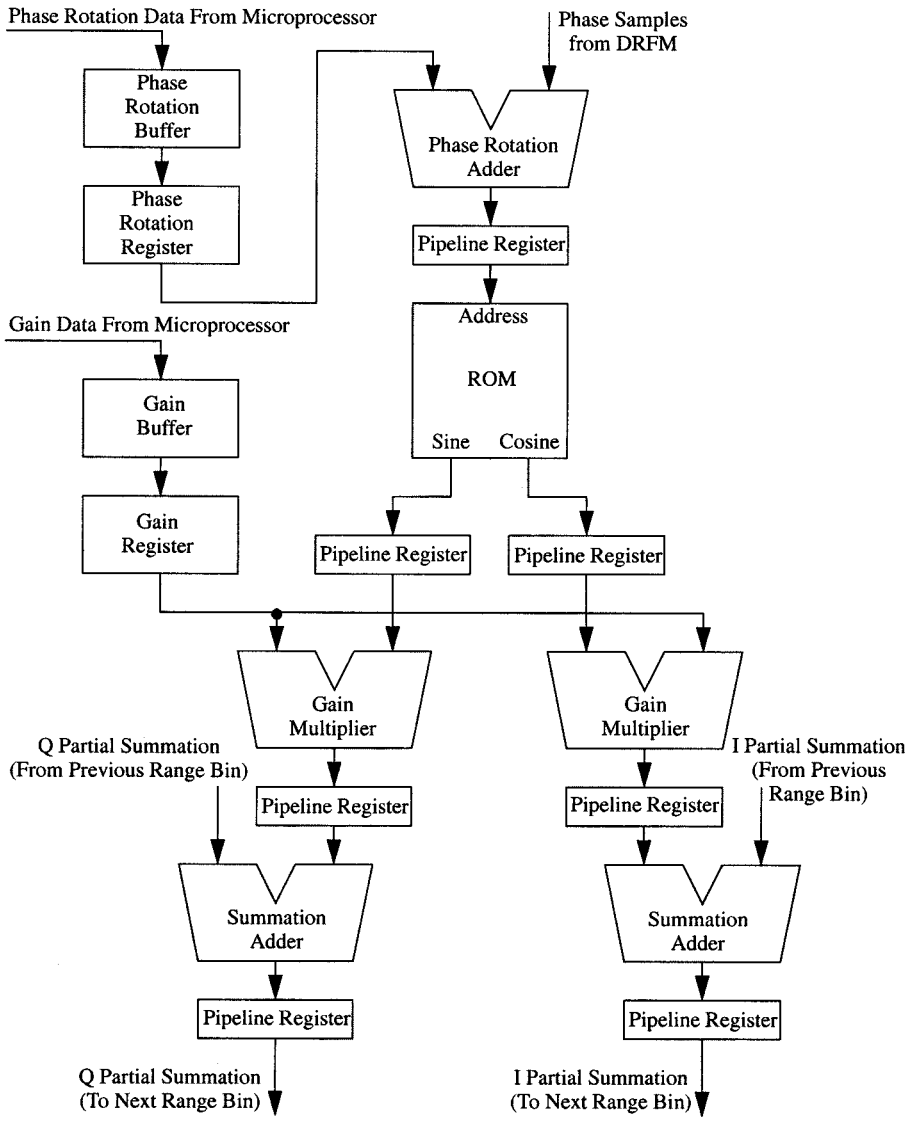

Fig. 6. Architecture of range-bin implementation.

With the design shown in Figs. 5 and 6, the clock speed of the DIS determines the range resolution of the false target image synthesized by the DIS because it determines the time delay between range bins. The resolution between range bins for the DIS can be calculated from

$$R_{\mathrm{R}} = \frac{C}{2f_{\mathrm{cl}}} \tag{7}$$

$$M_{\mathrm{SZ}} = R_{\mathrm{R}} \times N_{\mathrm{RB}} \tag{8}$$

where R_{R} is the range resolution, f_{cl} is the clock frequency, and C is the speed of light. For a typical DRFM/DIS system operating at 500 MHz, the range resolution is 0.3 m. Once the range resolution is known, (8) can be used to calculate the maximum size of the synthesized false target image, where M_{SZ} is the maximum target size and N_{RB} is the number of range bins. For a typical DIS with 512 range bins, the maximum size of the synthesized false target is 614 meters, providing the capability to synthesize false images of large ships such as aircraft carriers.

IV. Implementation

Initially, both field and mask programmable gate array technologies were investigated to implement the DIS design described in Section III. However, as previously explained, it is necessary to maintain a high clock frequency in order to have good range resolution of the synthesized false target image. Another advantage of maintaining a high clock speed is the reduced pipeline latency, which allows the synthesis of a false target closer to the platform containing the DIS system. In an actual deployed system, a clock speed of at least 500 MHz would be necessary. Another issue is the number of range bins on the DIS chip. The more range bins, the larger the synthesized false target image can be. In an actual deployed system, the number of range bins might need to be as large as 512 to generate a false target image of a ship such as an aircraft carrier. A chip containing 512 range bins and operating at clock speeds in excess of 500 MHz would not be possible with either field or mask programmable gate array technology. Therefore, a full-custom VLSI CMOS IC was proposed.

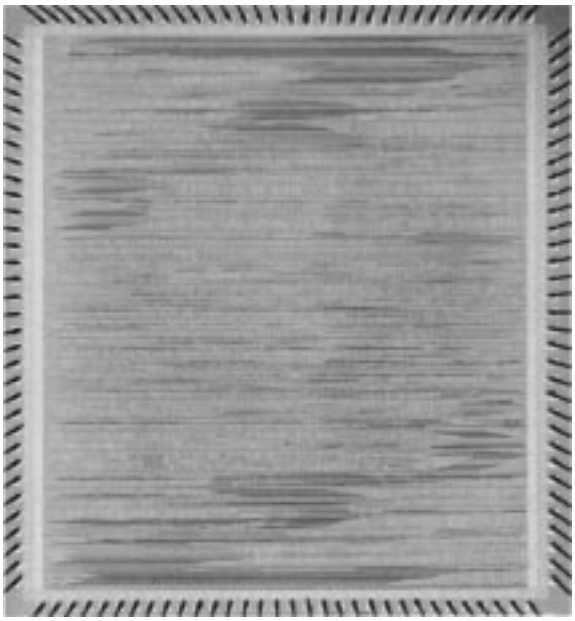

Fig. 7. Photograph of initial proof-of-concept implementation of DIS.

A full-custom VLSI CMOS DIS chip with 512 range bins would require over 6 million transistors and would need to be fabricated with a 0.18-μm or smaller process to obtain the required speed. Such a chip would be extremely expensive. To provide a proof-of-concept DIS at a reasonable cost, the initial implementation of the DIS described in this paper uses the design shown in Figs. 5 and 6 but with only eight range bins. However, multiple DIS ICs can be easily cascaded to create a system with as many range bins as desired. To reduce costs even further, the chip has been fabricated through the metal oxide semiconductor integration service (MOSIS) using the HP/Agilent 0.5-μm n-well process. The IC has a total of 81632 transistors, 79896 in the core and 1736 in the pad circuits. A photograph of the packaged die is shown in Fig. 7. The size of the core is approximately 5.1×5.6 mm. The size of the outside of the pad frame is approximately 5.5×6.1 mm. The IC was packaged in a 132-pin pin grid array (PGA) and has 126 I/O pins, two power pins, and two ground pins.

The IC shown in Fig. 7 was implemented using the Tanner Tools Pro IC design software package from Tanner Research and the standard 0.5-μm CMOS cell library supplied with the software. It should be noted that the cells in this library are not optimized for speed, power consumption, or layout area. However, they were used without modification to reduce the development time for this initial proof-of-concept IC. Furthermore, fully automatic cell placement and routing was used, also to reduce the design time. After the IC layout had been synthesized, several inefficiencies in the automatic cell place and route tool were discovered. It has been estimated that the clock speed and layout area of the IC could be improved by a factor of about 8 if optimized library cells and manual cell placement and routing were used. A reduction in power consumption would also be expected. Simulations indicate the use of optimized library cells, together with a high-performance 0.18-μm CMOS fabrication process, would allow the clock speed to reach 500 MHz, especially if the ripple-carry summation adder were replaced with a carry–lookahead adder. The ripple-carry summation adder is the slowest pipeline stage in the described design and is the limiting factor for clock speed. It should be noted that increasing the number of range bins from 8 to 512 would increase the size of the die, even if an optimized cell library, manual layout, and an 0.18-μm fabrication process were used.

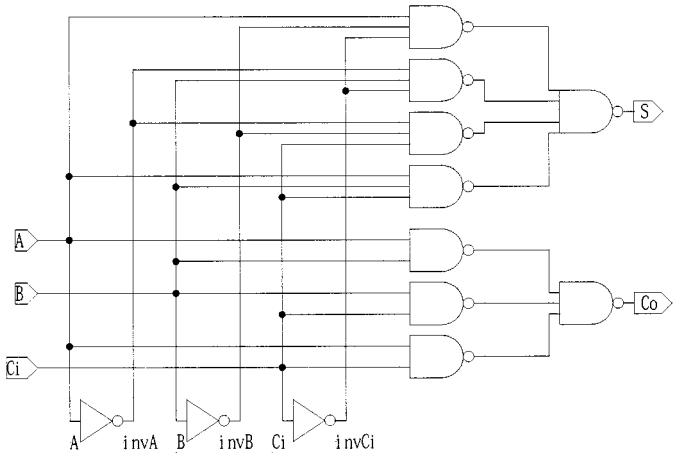

Fig. 8. Adder cell created from low-level logic system.

A ripple-carry adder was used to implement the summation adder in each range bin, instead of a high-performance carry–lookahead adder, to reduce the number of transistors and fabrication costs of the proof-of-concept IC. A 1-bit adder slice is shown in Fig. 8. To improve the speed of the circuit, a sum-of-products implementation was used. This circuit only has three logic gate delays from input to output, as opposed to the six logic gate delays for a traditional ripple-carry adder circuit that uses exclusive OR gates to initially generate a carry–generate signal and a carry–propagate signal, and then generate the sum and carry output signals from the carry–generate and carry–propagate signals.

Although the design shown in Fig. 8 is faster than a traditional ripple-carry adder, it also uses more logic gates. Using an adder cell built up from low-level logic gates proved to be somewhat inefficient. In future versions of the DIS, an optimized adder cell will be created and used to reduce the number of transistors, the size of the layout, and the logic propagation delays through the adders. The adder shown in Fig. 8 requires a total of 56 transistors and has three logic gate delays. It is possible to construct an adder cell using only 32 transistors and having only two logic gate delays. In a DIS with 512 range bins, this is a savings of 454656 transistors. The speed of the adder cell shown in Fig. 8 and the speed of the 16-bit carry propagate summation adders that use it limit the clock speed of this initial proof-of-concept DIS to less than 100 MHz.

Gain multiplication within each range bin is accomplished using two stages of 2-to-1 multiplexers, as shown in Fig. 9. The number of transistors and the layout area could have been reduced, although at the expense of increased design time, by implementing the multiplier with a single-stage barrel shifter implemented with pass-gate logic. The gain multiplier shown in Fig. 9 uses 220 transistors and is used twice in each range bin. A single-stage barrel shifter implemented with pass-gate logic

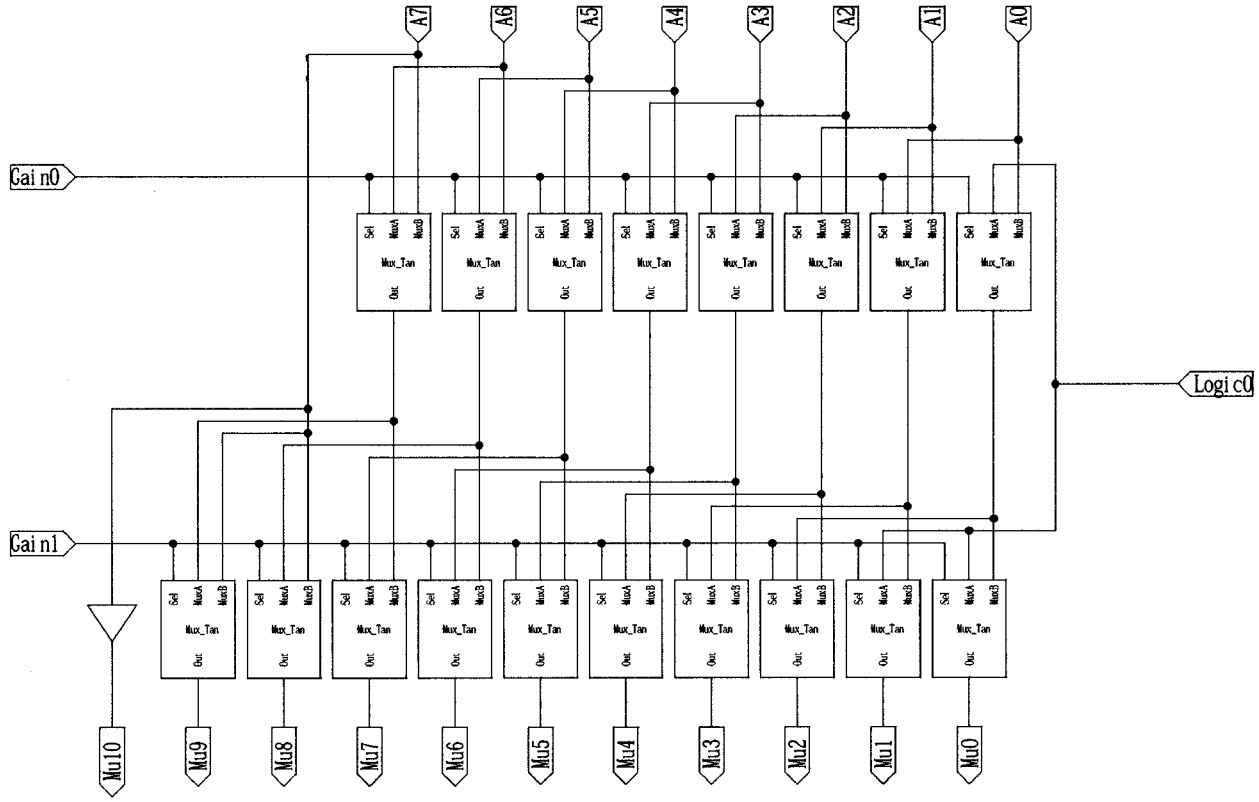

Fig. 9. Gain multiplier created from 2-to-1 multiplexers.

would require only 112 transistors and would save a total of 110592 transistors in a 512 range bin DIS chip.

Within each range bin, phase samples are transformed into amplitude signals using the sine and cosine operations. After considering various different design tradeoffs, it was decided that a lookup table would require the least amount of transistors and would provide the greatest speed for implementing these functions. The sine and cosine tables were combined into a single 32-address-by-16-bit ROM. To reduce the number of required transistors, the ROM uses the same address decoding logic for both the sine half and the cosine half.

The actual matrix of memory cells in the ROM is composed of both nFET pulldown transistors and pFET pullup transistors. This is a departure from typical ROM design. Usually, a ROM cell will contain an nFET pulldown transistor if it is programmed with a logic 0, but will not contain anything if it is programmed with a logic 1. When a cell is addressed that does not contain any transistor, a logic 1 is generated on the bit line by a pFET pullup transistor attached to the bit line. Fig. 10(a) illustrates a typical ROM. The cell on the left is programmed with a logic 0 and the cell on the right is programmed with a logic 1. However, ROMs implemented using this type of circuit can have slow output rise and fall times. When the output is falling, the nFET pulldown must sink the current sourced by the pFET pullup on the bit line as well as the discharge current for all parasitic capacitance on the bit line. When the output is rising, the pFET pullup on the bit line is not able to source as much current as the larger switched pFET in Fig. 10(b). Fig. 10(b) shows two memory cells from the ROM matrix in the DIS IC. The cell on the left is programmed with a logic 0 and contains an nFET pulldown transistor. The cell on the right is programmed with a logic 1 and contains an active pFET pullup transistor. The bit lines do not have any pullup transistors. This design greatly improves the speed of the ROM, as can be seen by the T-SPICE simulation output shown in Fig. 11. This simulation run was done using transistor parameters extracted from actual devices. As can be seen from Fig. 11, address access time is in the vicinity of 2.5 ns. Furthermore, the low-to-high and high-to-low output transitions are fairly well matched.

V. Simulations and Results

The software package used does not include a logic-level simulator such as Verilog or VHDL, although is does have a VHDL interface. However, this interface was not used for this project, and all simulations of the implementation were performed with T-SPICE, the Tanner Research proprietary SPICE-like circuit simulator that is a part of Tanner Tools Pro. Transistor parameters extracted from previous fabrication runs were supplied by the fabrication service, thus ensuring reasonable accuracy for speed and power simulations. Simulations indicate a maximum clock speed of 66 MHz, including an allowance for sufficient clock margins. As mentioned previously, the limiting factor is the ripple-carry chain in the 16-bit summation adders. Simulations indicate average power consumption of approximately 0.41 W with a 3.3-V power supply, including 0.11 W in the core and 0.30 W in the pad frame. Peak power consumption occurs during the rising edge of the clock and is approximately 1.58 W with a 3.3-V power supply, including 0.53 W in the core and 1.05 W in the pad frame. The low I/O power, relative to the

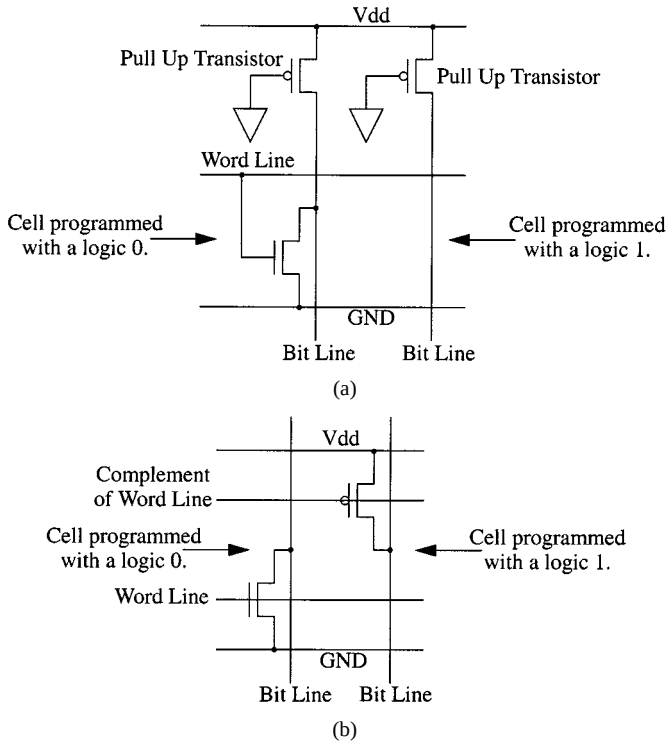

Fig. 10. (a) Traditional ROM cells with active pulldown and bit line pullup. (b) ROM cells used in the DIS with active pulldown and active pullup.

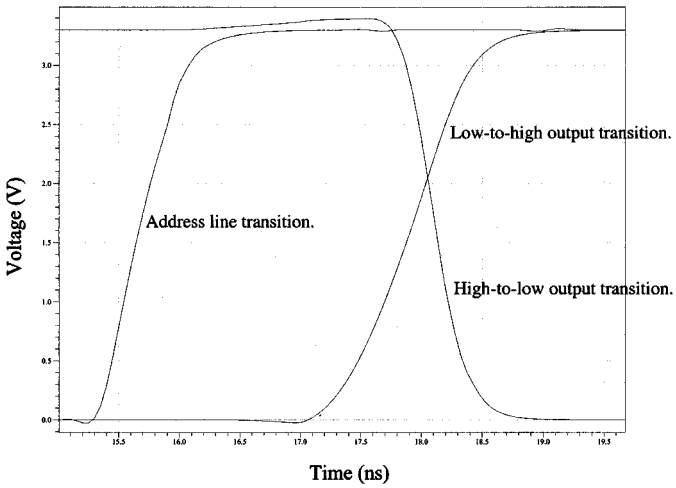

Fig. 11. T-SPICE simulation output of sine/cosine lookup table ROM.

number of inputs and outputs, is partly because only 36 of the 126 I/O pins are output pins and partly because of the use of low-power output drivers. The low-power output drivers are not as fast at higher power drivers, but they are sufficient for this IC design that has a limited clock speed because of the logic core.

When simulating larger components at higher levels of the hierarchical design, and especially when simulating the entire IC, a large number of bits need to be checked over a large number of clock cycles to ensure correct functionality. Specifically, on every clock cycle, all 16 bits of both the I and the Q outputs need to be checked. To speed up result analysis and prevent analysis errors, this process was automated. The T-SPICE output was directed to a file which was then post-processed with a MATLAB [14] program. The MATLAB program reads the output voltages and converts them to logic levels via a threshold algorithm. It then compares the bit patterns against MATLAB simulation output for the same input test vectors.

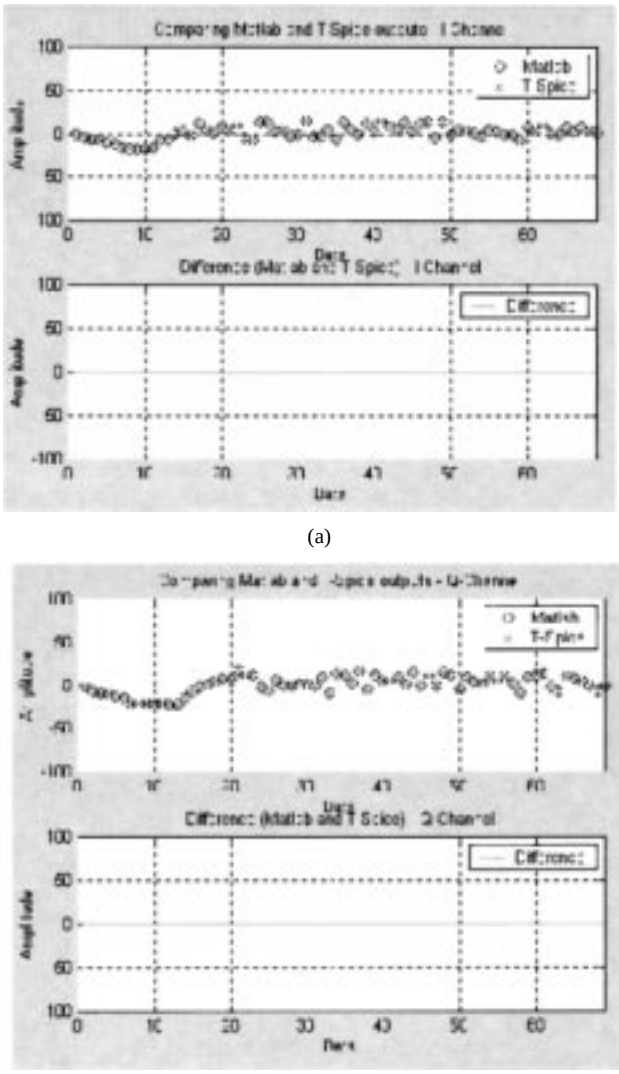

Fig. 12. (a). I-channel Matlab versus T-SPICE (b). Q-channel Matlab versus T-SPICE.

An example of the comparison output is shown in Fig. 12(a) and (b). It can be seen from this figure that the T-SPICE simulation output of the circuit extracted from the layout perfectly matches the MATLAB simulation output. The input vector for this test includes approximately 60 digitized samples of a single radar pulse. For this test, the DIS is programmed to synthesize a false target radar image of the USS Crockett, shown in Fig. 1(a). With only eight range bins, a single proof-of-concept DIS chip is not capable of generating the resolution seen in Fig. 1(b). Multiple chips would need to be cascaded together to achieve this resolution. However, a single chip is still capable of generating a realistic false target radar image. Fig. 13 shows what a single DIS chip is capable of generating. This image was generated by a Matlab simulation of the eight-range-bin DIS chip programmed to emulate 26 scattering surfaces and assuming 64 radar pulses. The hull, bridge, quarter deck, and forward and aft masts are all distinguishable.

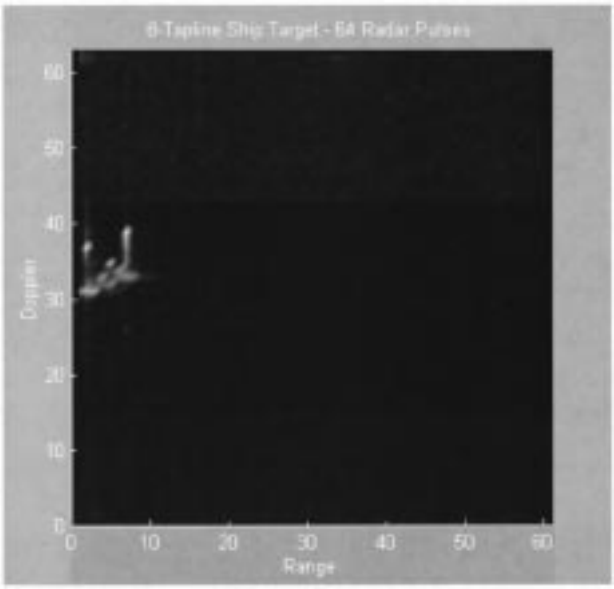

Fig. 13. False target radar image of USS Crockett generated by proof-of-concept DIS IC with eight range bins.

VI. Testing and Results

After fabrication, functional testing was conducted in the Advanced Microelectronics and VLSI Systems Laboratory in the Department of Electrical and Computer Engineering at the U.S. Naval Postgraduate School, Monterey, CA. Initial testing was conducted at a moderate clock speed of 10 MHz using a Hewlett Packard 16500B logic analyzer equipped with a network interface and several of the optionally available test vector generation boards. The input test vectors used were the same test vectors that were used for conducting the T-SPICE simulations of the entire IC before fabrication. Input vectors were first downloaded into the HP 16500B via the network interface. After executing a test, the captured results were uploaded back to a host PC for analysis with the same MATLAB program that was used for analyzing the results of the T-SPICE simulations of the entire IC before fabrication.

Initially, all 25 of the packaged ICs were confirmed to be 100% functional. At this point, 16 of the ICs were shipped to the U.S. Naval Research Laboratory, Washington, DC, for incorporation into an electronic countermeasures test bed. Testing continued on some of the remaining ICs at the Naval Postgraduate School. All of these chips worked correctly up to a maximum speed of 71 MHz, slightly greater than the 66-MHz maximum speed predicted by the T-SPICE simulations. Average power consumption was measured at 0.132 W at 70 MHz with a 3.3-V power supply. This is 0.278 W lower, or 32% of, the average power consumption estimated from T-SPICE simulations. We attribute this difference to a lower percentage of logic gates and flip-flops switching on each clock transition than the original 50% estimate. A 50% estimate was originally used because all simulations were done with a circuit simulator (T-SPICE) which, like most other circuit simulators and versions of SPICE, does not have the ability to calculate the number of logic gates that transition on each clock.

VII. Conclusion

This paper has described the theory, design, implementation, simulation, and testing of an ASIC capable of generating false target radar images for countering wideband synthetic aperture and inverse synthetic aperture imaging radars. An introduction to the application and operation of the ASIC in an electronic attack system has also been presented. The IC has been fabricated and tested and found to be fully functional at a nominal operating speed of 66 MHz with reasonable clock margins. The chip is currently being integrated into an electronic attack test bed at the U.S. Naval Research Laboratory.

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References

[1] D. R. Wehner, *High-Resolution Radar*, 2nd ed. Boston, MA: Artech, 1995, ch. 1.
[2] R. M. Nuthalapati, "High resolution reconstruction of ISAR images," *IEEE Trans. Aerospace Electron. Syst.*, vol. 28, pp. 462–472, Apr. 1992.
[3] Z. S. Liu, R. Wu, and J. Li, "Complex ISAR imaging of maneuvering targets via the Capon estimator," *IEEE Trans. Signal Processing*, vol. 47, pp. 1262–1271, May 1999.
[4] B. Zheng, S. C. Yin, and X. Mengdao, "Principles and algorithms for inverse synthetic aperture radar imaging of maneuvering targets," in *Record IEEE 2000 Int Radar Conf*, May 2000, pp. 316–321.
[5] R. Voles, "Resolving revolutions: Imaging and mapping by modern radar," *IEE Electron. Commun. Eng. J.*, vol. 5, no. 1, pp. 3–12, Feb. 1993.
[6] M. T. Fennell and R. P. Wishner, "Battlefield awareness via synergistic SAR and MTI exploitation," *IEEE Aerospace Electron. Syst. Mag.*, vol. 13, pp. 39–45, Feb. 1998.
[7] S. Y. Yeo, "A digital image synthesizer for ISAR counter targeting," Master's thesis, U.S. Naval Postgraduate Sch., Monterey, CA, 1998.
[8] J. M. Nasr and D. Vidal-Madjar, "Image simulation of geometric targets for spaceborn synthetic aperture radar," *IEEE Trans. Geosci. Remote Sensing*, vol. 29, pp. 986–996, Nov. 1991.
[9] S. Y. Wang and S. K. Jeng, "Generation of point scatterer models using PTD/SBR technique," in *IEEE Antennas and Propagation Soc. Int. Symp. 1995 Dig.*, vol. 4, June 1995, pp. 1914–1917.
[10] B. Haywood, W. C. Anderson, J. T. Morris, and R. Kyprianov, "Generation of points catterer models for simulating ISAR images of ships," in *Radar97 Conf. Proc.*, Oct. 1997.
[11] D. R. Wehner, *High-Resolution Radar*, 2nd ed. Boston, MA: Artech, 1995, ch. 4.
[12] S. R. T. Ekestorm and C. Karow, "An all-digital image synthesizer for countering high-resolution imaging radars," joint Master's thesis, U.S. Naval Postgraduate Sch., Monterey, CA, 2000.
[13] B. Parhami, *Computer Arithmetic, Algorithms and Hardware Designs*. New York: Oxford Univ. Press, 2000, ch. 8.
[14] *MATLAB Reference Manual and User's Guide*, The MathWorks Inc., Natick, MA, 2000.

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